Exhibit O

REDACTED
IN ITS ENTIRETY

Exhibit P

REDACTED
IN ITS ENTIRETY

Exhibit Q

ORRICK

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July 7, 2005

Bas de Blank
(650) 614-7343
bdeblank@orrick.com

VIA FACSIMILE AND U.S. MAIL

Gina M. Steele
Fish & Richardson P.C.
500 Arguello Street
Suite 500
Redwood City, CA 94036

Re: Power Integrations v. Fairchild Semiconductor et al. (CA 04-1371 JJF)

Dear Gina:

Your letter of June 1, 2005 requested dates for the deposition of Fairchild Semiconductor International employees in Korea. Neither Fairchild Semiconductor International, Inc. nor Fairchild Semiconductor Corporation – the two defendants in this action – have employees in Korea. Specifically, Messrs. E.S. Kim, "K.W." Jang, Y.C. Ryu, and C.S. Lim are employed by nonparty Fairchild Korea Semiconductor Ltd. Thus, Fairchild has no obligation to produce these witnesses for deposition in Korea or anywhere else.

As you know, we believe that many of deposition topics outlined in your letter – including topics seeking information concerning damages prior to the filing of the complaint or sales and customer outside of the United States – are overly broad, unduly burdensome, and not calculated to lead to the discovery of relevant information. While we will formally object once Power Integrations serves an actual deposition notice, pursuant to Federal Rule of Civil Procedure 30(b)(6) – and subject to appropriate objections concerning the scope of the deposition topics -- Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation will designate an appropriate person or persons to testify as to matters known by either of the parties.

The precise witness for each topic will depend on the final wording of the topic. Thus, as we previously suggested, we propose that Power Integrations provide a draft of the deposition notice it intends to serve. Once we receive it, we will determine the appropriate witness or witnesses and provide the dates they are available. Once the parties agree to the dates, Power Integrations can serve a formal deposition notice if it chooses. We will, of course, do the same with deposition notices to Power Integrations.

Based on the outline of topics provided by Power Integrations, it is highly likely that some or all of the witnesses will need to be deposed in Korea. As we have explained, we have a conflict with the proposed dates of August 4-11, 2005 but the Korean witnesses will be available September 1, 2, and 5-10, 2005. Once we have the final wording of the deposition topics and can identify the

ORRICK

appropriate witness, we will inform Power Integrations whether they are located in the United States or abroad and whether they will require a translator.

You requested that the deposition of any Korean witness related to sales and marketing of the Fairchild devices and Fairchild's knowledge of the Power Integrations patents occur during the week of September 12, 2005. As I indicated, we are checking the availability of the likely witness and will let you know as soon as possible.

Sincerely,

Bas de Blank

Encl.

cc: William J. Marsden, Jr.
Howard G. Pollack

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FAX TRANSMISSION

DATE July 8, 2005

NO. OF PAGES (INCLUDING COVER SHEET) 3

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Bas de Blank	650-614-7343

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name	company/firm	tel	fax
Gina M. Steele	FISH & RICHARDSON P.C.		650.839.5071
CC			
William J. Marsden, Jr.	FISH & RICHARDSON P.C.		302.652-0607
Howard G. Pollack	FISH & RICHARDSON P.C.		650.839.5071

RE *Power Integrations v. Fairchild Semiconductor et al*

MESSAGE

Please see attached.

C-M-A 10414-25/7584 Originals Will Follow

IF YOU DO NOT RECEIVE ALL PAGES, PLEASE CALL MIMI SAGMIT AT (650) 614-7451 AS SOON AS POSSIBLE.

DOCSSV1:409340.1
10414-25 MZB/S77

Exhibit R

Jennifer Pierce

From: Kristina Kim [kristinas.kim@samsung.com]
Sent: Friday, December 16, 2005 11:32 AM
To: Michael Headley
Cc: basdeblank@orrick.com; ???
Subject: Fwd: Power Integrations v. Fairchild
Attachments: LG Electronics order.pdf; LG Electronics opinion.pdf; Memorandum Order.pdf

Mike --

I am doing a quick e-mail informing you that, pusuant to explanation I received from counsel for Fairchild (forwarded below), Samsung International, Inc. (SII) has not purchased from Fairchild the part items you list in your Subpoena, as further amended in your discovery responses produced to Fairchild in this lawsuit.

Also, I confirm that SII has at no time purchased components from System General.

Our formal repsonse to the Subpoena will be sent to you during January 2006.

Regards,

Kristina Sojung Kim, Esq.
General Counsel
Samsung International, Inc.
Office (619) 671-6011
Fax (619) 671-6010/6013
Cell (619) 384-5685
E-mail: kristinas.kim@samsung.com

------- **Original Message** -------
Sender : de Blank, Bas<basdeblank@orrick.com>
Date : 2005-12-13 15:13
Title : Power Integrations v. Fairchild
Kristina,

It was good to speak with you. As we discussed, while Power Integrations originally accused Fairchild's FSCQ0765 device, in its latest (September 30, 2005) interrogatory response on the subject, Power Integrations has dropped those accusations and no longer accuses the FSCQ0765 device of infringing any of its patents. Thus, whether or not Fairchild sold any of its FSCQ0765 devices to Samsung is not of any relevance to this case.

Further, I have attached a copy of the Court's Order precluding Power Integrations from seeking damages related discovery prior to the filing of the complaint. The relevant passage of that Order is on page 6, which states "Accordingly, the Court concludes that Power Integrations has not established that documents related to Fairchild's sales prior to the date of the Complaint are relevant to the question of damages, and therefore, the Court concludes that Power Integrations is not entitled to the discovery of these documents." As the Order notes, the Complaint was filed on October 20, 2004. Thus, Samsung need not produce any sales or other information prior to October 20, 2004.

I also attach a copy of the Court's Order quashing an essentially identical subpoena Power Integrations served on LG.

I will also send you copies of these orders via facsimile.

I hope that this answers all of your questions. I understand that Samsung intends to respond that Samsung has not purchased any accused Fairchild device. If that is not correct or if there is anything else I can do to be of assistance, please do not hesitate to call.

Bas de Blank
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1000 Marsh Road
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650-614-7401 (fax)

From Orrick, Herrington & Sutcliffe LLP <orrick.com> on 12/13/2005 03:14:23 PM
IRS Circular 230 disclosure:
To ensure compliance with requirements imposed by the IRS, we inform you that any tax advice contained in this communication, unless expressly stated otherwise, was not intended or written to be used, and cannot be used, for the purpose of (i) avoiding tax-related penalties under the Internal Revenue Code

or (ii) promoting, marketing or recommending to another party any tax-related matter(s) addressed herein.

==========

Exhibit S

ORRICK, HERRINGTON & SUTCLIFFE LLP
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October 17, 2006

Brian H. VanderZanden
(650) 614-7629
bvanderzanden@orrick.com

VIA ELECTRONIC MAIL

Howard G. Pollack
Fish & Richardson P.C.
500 Arguello Street, Suite 500
Redwood City, CA 94036

Re: Power Integrations v. Fairchild Semiconductor et al. (CA 04-1371 JJF)

Dear Howard:

We have learned that non-party Intersil has additional materials corroborating James Beasom's conception and reduction to practice of his '173 patent. These materials include prototype wafers, packaged prototype chips, and travelers and bond diagrams describing the process conditions of the prototypes. As soon as we obtain these materials, we will produce or make them available to Power Integrations.

Sincerely,

Brian H. VanderZanden

BHV:ma5

cc: William J. Marsden, Jr.
Frank E. Scherkenbach

Exhibit T

ORRICK

ORRICK, HERRINGTON & SUTCLIFFE LLP
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April 24, 2006

Brian H. VanderZanden
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bvanderzanden@orrick.com

VIA FACSIMILE

Michael R. Headley
Fish & Richardson P.C.
500 Arguello Street, Suite 500
Redwood City, CA 94036

Re: Power Integrations v. Fairchild Semiconductor et al. (CA 04-1371 JJF)

Dear Michael:

As I mentioned in my previous letter, Fairchild is working with Intersil to collect any non-privileged documents Intersil may have that are relevant to Power Integrations' discovery requests. Please find the attached documents bearing Bates range FCS1691462 - FCS1691473, all marked Highly Confidential. We received a poor quality copy of these documents Friday, and did not receive a higher quality copy until today. They were not previously in our possession, custody, or control.

Please feel free to contact me with any issues concerning these documents, or any other Intersil documents.

Sincerely,

B. VanderZanden

Brian H. VanderZanden

BHV:ma5

cc: William J. Marsden, Jr.
Howard G. Pollack

HARRIS SEMICONDUCTOR SECTOR

TO: T. N. Twomey	FROM: J. D. Beason	DATE: 12/3/84

SUBJECT: Patent Disclosure SE-395

Please find attached a disclosure "A High Voltage Lateral MOS Structure with Reduced On Resistance". Devices of the disclosed type have been designed and included in a test mask set. They may be used in future high voltage analog switch and multiplexer products.

J. D. Beason

JDB:dg

M124

INVENTION CHECKLIST

Instructions: This form is to be used for initial reporting of invention to Division Counsel. Items 1-9 should be completed. Check applicable block(s) in items 3-7. Item 10 will be completed by Counsel and copy returned to Preparer.

1. Date of first written description of the invention: 4/10/84

2. Subject of invention: A high voltage lateral MOS structure with reduced on resistance.

3. Principal category:

- [ ] Process
- [x] Device
- [ ] Circuit
- [ ] Other

4. Current status:

- [ ] Concept only
- [x] Experimental work begun
- [ ] Reduced to a practical embodiment

5. Priority:

- [ ] High
- [x] Moderate
- [ ] Low

6. Usage:

- [ ] Proposed for use in HSD product
- [ ] Currently used in HSD product
- [x] Other

7. Date of first publication, offer of sale, or commercial use:

None.

8. Person(s) to contact for additional information:

J. D. Beasom 7567
Telephone Ext.

Telephone Ext.

9. Person who prepared this report:

J. D. Beasom

10. Receipt acknowledged by Counsel:

Date:

A High Voltage Lateral MOS Structure

With Reduced On Resistance

The lateral drift region MOS structure illustrated in Fig. 1 is a known structure which can be used to build high voltage MOS devices. The basic high voltage junction of the structure is the drain body junction.

The drift region is used to connect the high voltage part of the structure to the gate and source which never assume large voltages with respect to the body. The drift region acts as a JFET channel with the underlying MOS body acting as JFET gate. It is designed to totally deplete as the drain body is reverse biased before critical field is reached in the channel to body depletion layer. In this way the drain body breakdown voltage is preserved and the source and gate over gate oxide are shielded from high drain body voltage by the pinched off JFET channel.

The resistance of the lateral drift region JFET channel is in series with the MOS channel resistance, consequently the channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltage, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

The structure described in this disclosure provides the desired reduced channel resistance. The reduction in channel resistance is accomplished by addition of a top gate which lies over the channel to the prior art structure and is illustrated in Fig. 2. The top gate allows total channel doping to be increased because the top gate to channel depletion layer holds some channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. This additional channel charge (ionized channel impurity atoms) causes the reduction in channel resistance.

The top gate must be designed differently than a normal JFET gate. It must be totally depleted at a body (to which it is connected) drain voltage below the breakdown voltage of the junction it forms with the drain which it abuts. It must also totally deplete before the body to channel depletion layer reaches the top gate to channel depletion layer, thus insuring that a large top gate to drain voltage is not developed by punch through action from the body. A normal JFET gate never totally depletes under any operating conditions.

The channel of the JFET drift region must contact the inversion layer MOS surface channel where they meet. One way to achieve this is illustrated in Fig. 3. The top gate and channel are formed by ion implant using an angled implant mask at the channel edge. The angled mask edge causes the channel and top gate implants to curve to the surface as they are progressively retarded by the increasing thickness of the implant mask. Thus the channel comes to the surface beyond the end of the top gate.

A High Voltage Lateral MOS Structure With Reduced On-Resistance

Another method to bring the channel into contact with the surface uses diffusion. The channel and top gate are diffused (possibly after deposition by ion implant). The doping levels and diffusion times are chosen such that the channel diffuses beyond the end of the top gate and reaches the surface. This approach can be facilitated by choosing a top gate dopant which has a lower diffusion coefficient than that of the channel.

The top gate should be tied to the body which is the bottom gate of the drift region JFET. A particularly effective way to accomplish this is to overlap the end of the drift region near the MOS channel with the body contact region. To be effective the body contact must be higher in concentration than the channel so that it forms a continuous region horizontally and/or vertically to the body region.

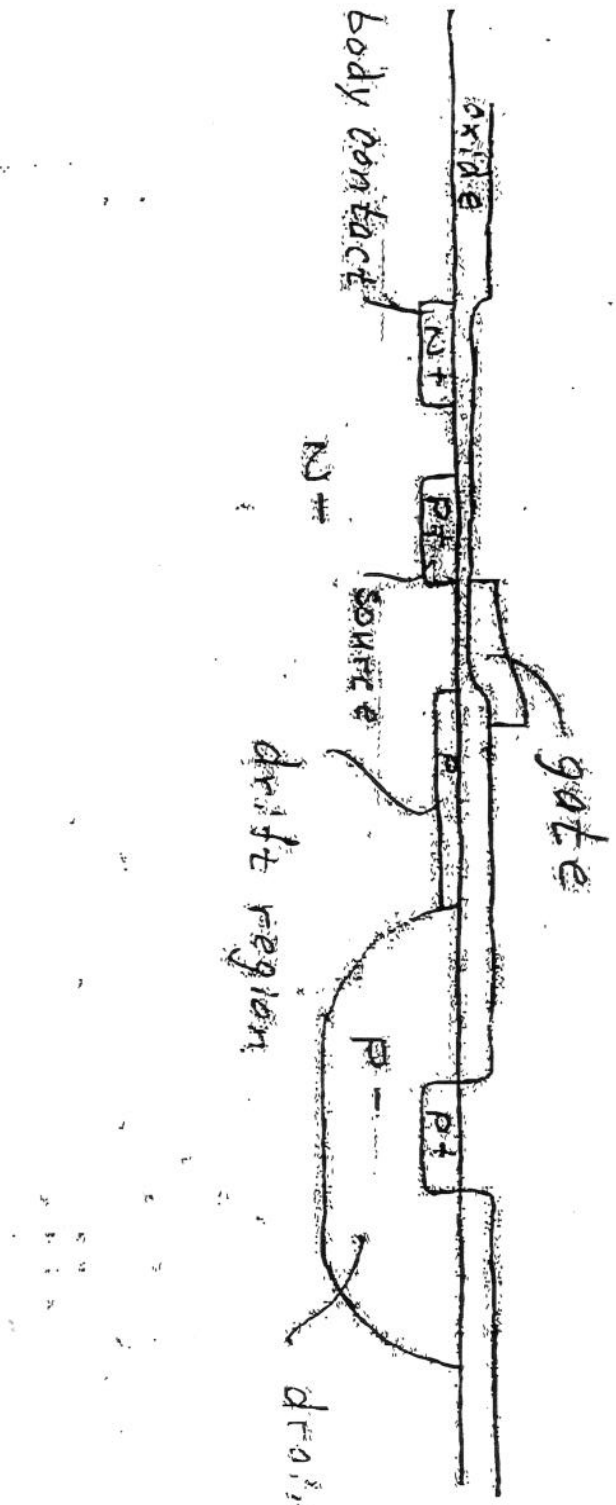


Fig 1

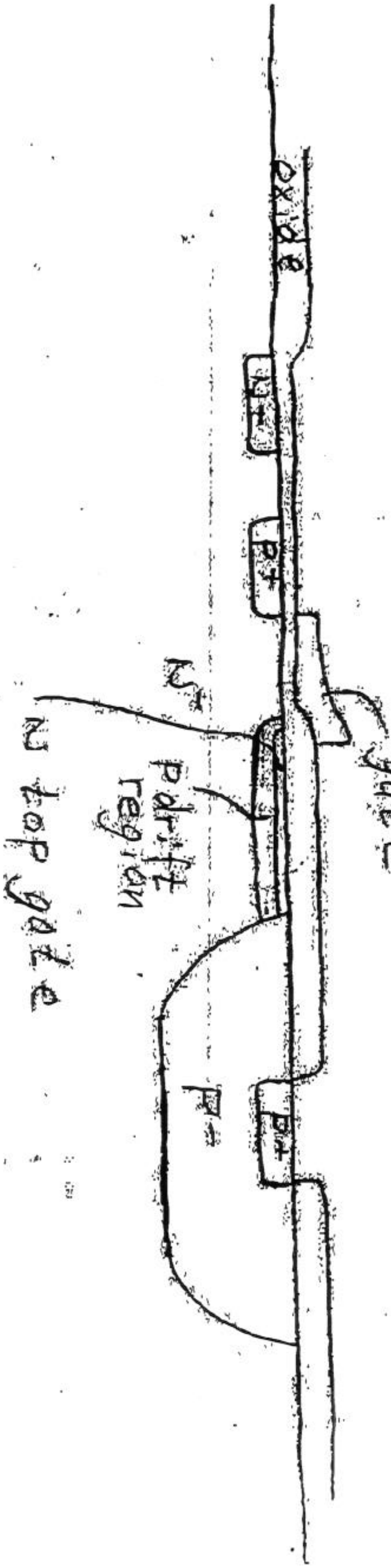
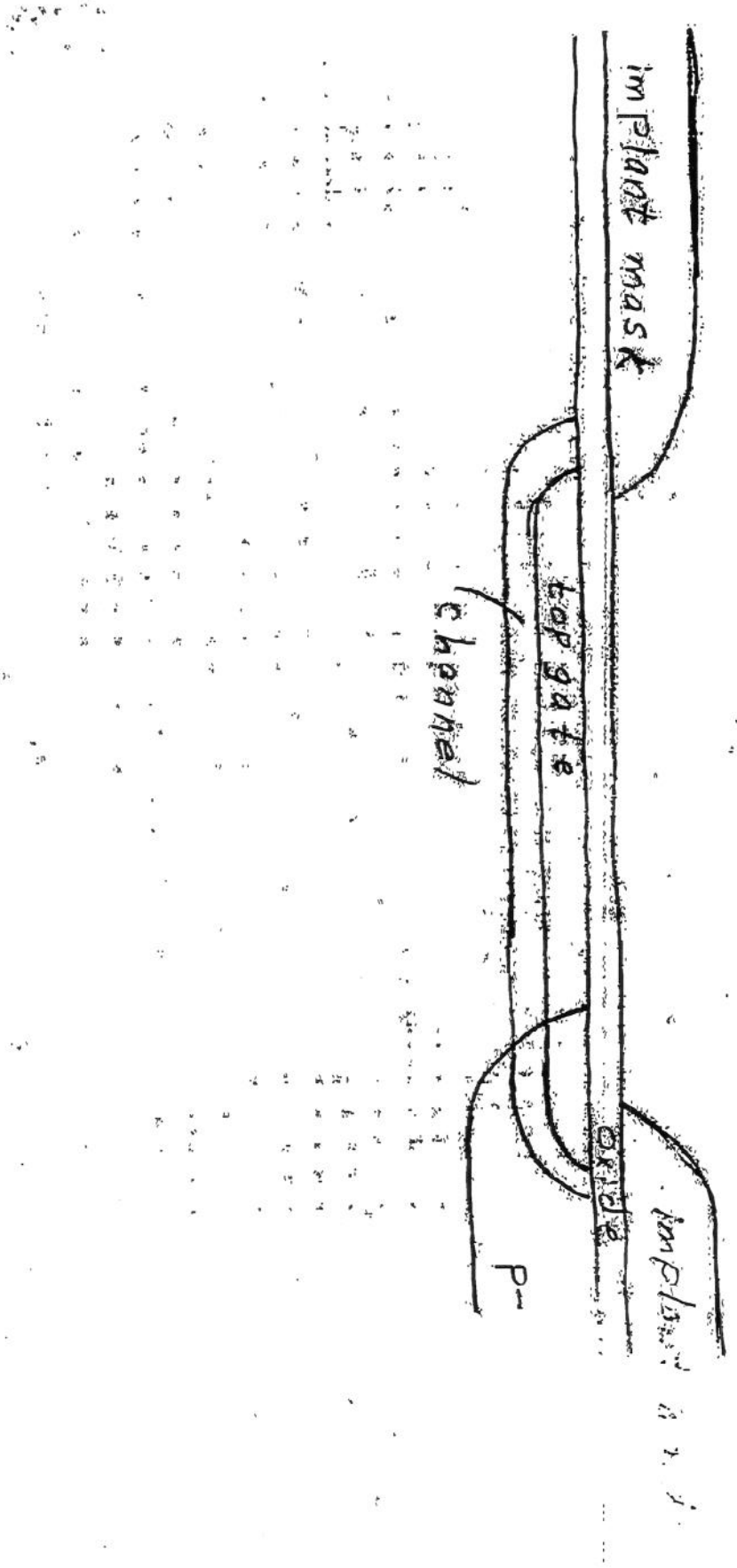


Fig 2


main mast
top gate
channel
Fig 3

HARRIS

SEMICONDUCTOR SECTOR

0681V-JDB-28030

TO:	FROM:	DATE:
T. N. Twomey	J. D. Beasom	4/24/85

SUBJECT: Broadening of Parent Disclosure SE-395 "A High Voltage Lateral MOS Structure"

The disclosure describes an improvement to lateral drift region type MOS devices. Lateral transistors can also be made using a similar lateral drift region. Such devices are described in the U.S. patents of Sirsi (4,284,236) and Sugawara et al (4,419,685).

The same modification which I have disclosed to improve the MOS device can be used to improve the lateral bipolar device. All the same design and structure considerations apply. Fig. 1 illustrates a prior art device and one with the improvement of my disclosure. Fig. 2 illustrates an improved device in which the drift region does not extend all the way to the N emitter shield. The device can also be made as shown in Fig. 2 but with the emitter shield deleted.

Also illustrated in Fig. 2 is use of a deep diffusion to form the collector. This leads to higher breakdown voltage. Either the emitter step (as shown in Fig. 1) or a special step (as shown in Fig. 2) may be used to form the collector. The same is true for source and drain for the MOS device described in the original disclosure. The choice made will depend upon the desired device performance and does not affect the concept of the disclosure.

An extension of the concept which may be used to increase drain-body breakdown for the MOS and collector-base breakdown for the bipolar device is shown in Fig. 3. The drift region extends outward from the entire perimeter of the drain or collector. In this case, it acts to mitigate the breakdown reduction due to junction curvature.

Planar diode breakdown improvement by use of a surface layer of the conductivity type of the surface region (drain or collector in these examples) which extends out from the perimeter of that layer is known prior art. The improvement here is that a common set of process steps produces both a suitable breakdown improvement layer (here N over P or P over N rather than prior art single conductivity type) and an improved drift region.

J. D. Beasom

JDB:dg

M124

fig 1

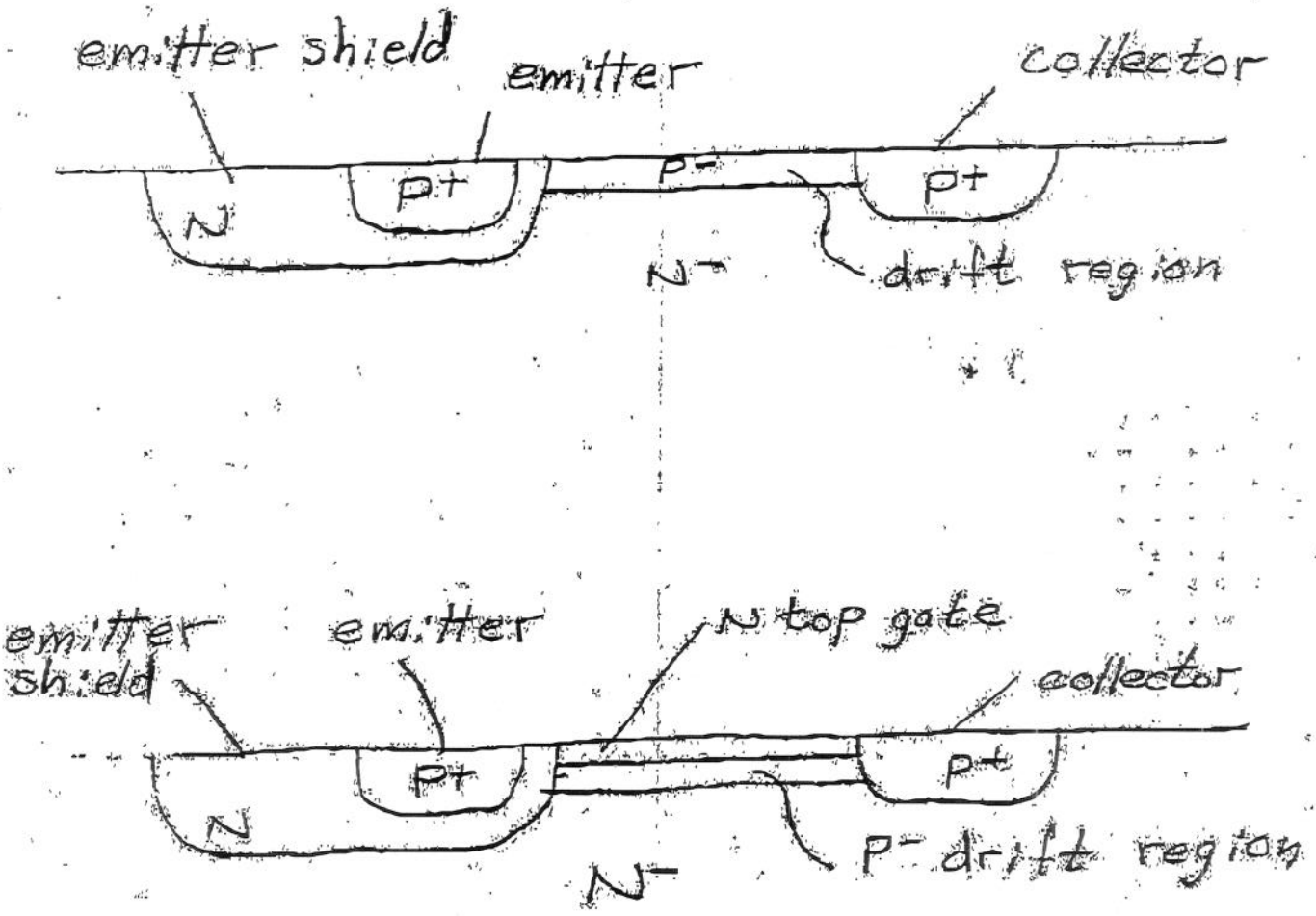

emitter shield
emitter
collector
P+
P-
P+
N
N-
drift region
emitter shield
emitter
N top gate
collector
P+
P+
N
N-
P- drift region

fig 2

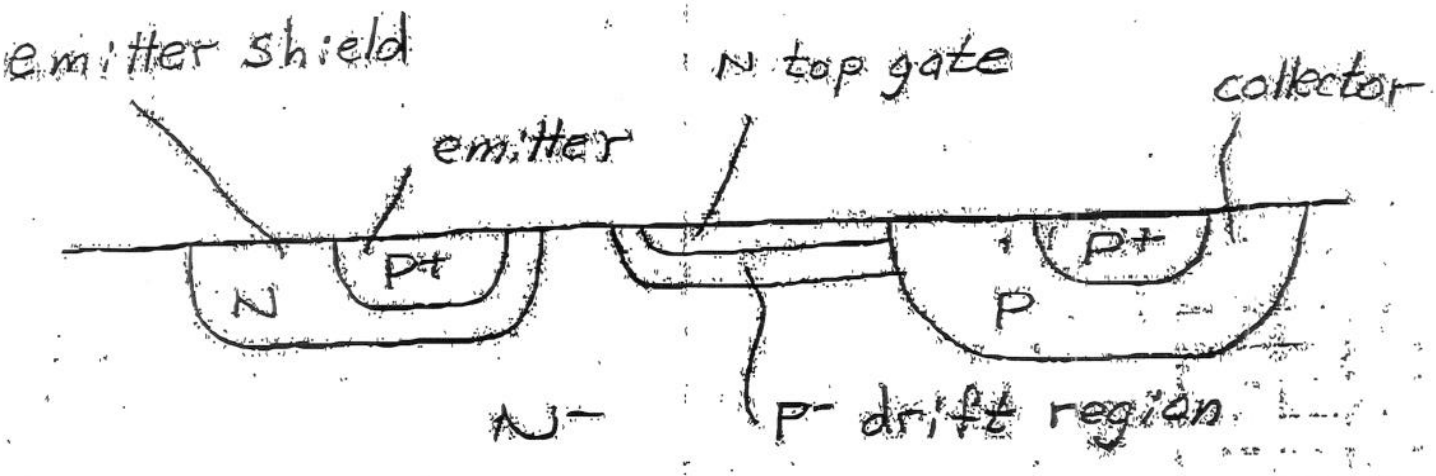
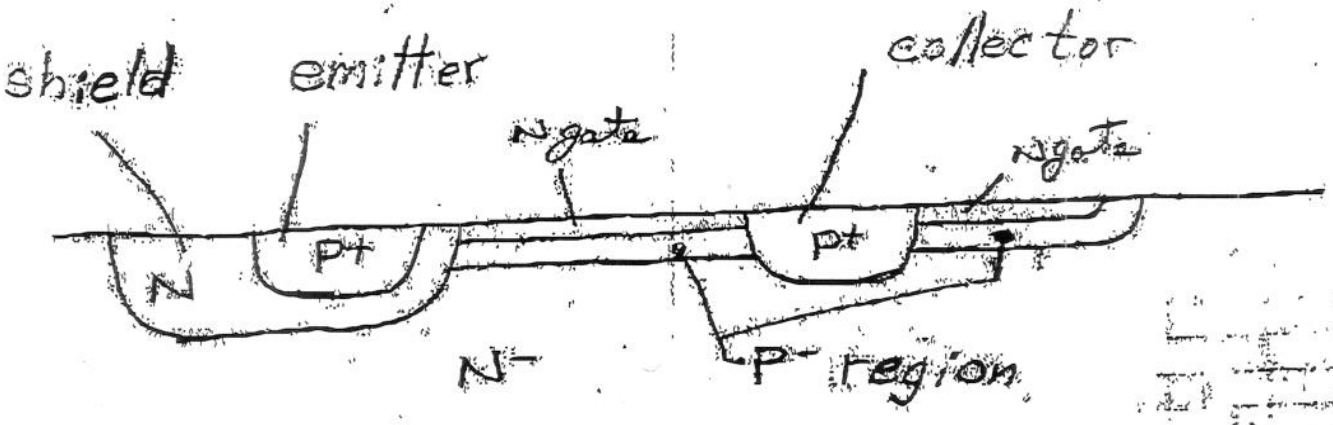
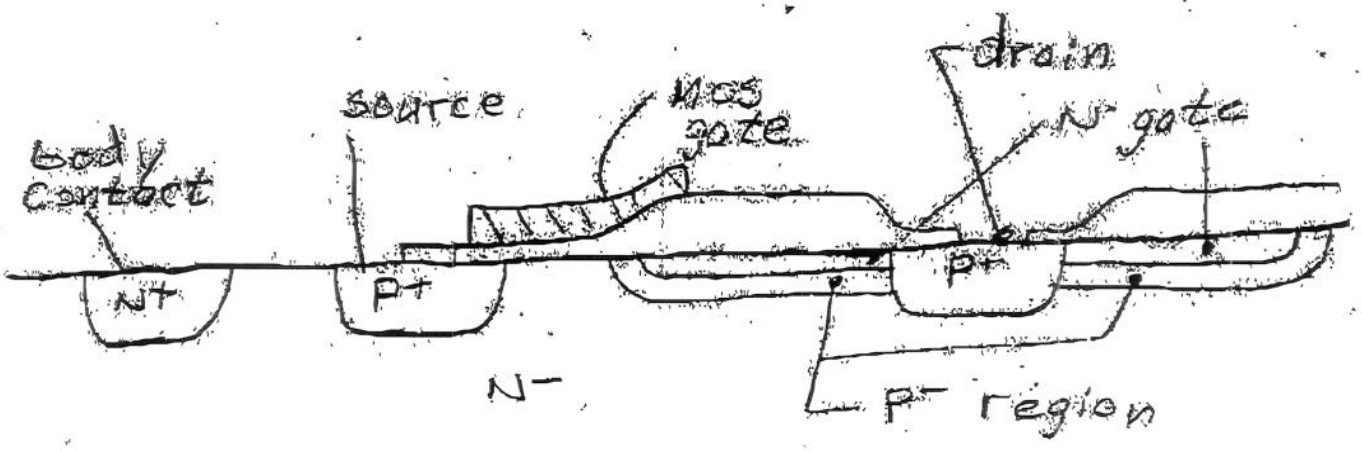

emitter shield
emitter
N top gate
collector
N
P+
P+
P
N-
P- drift region

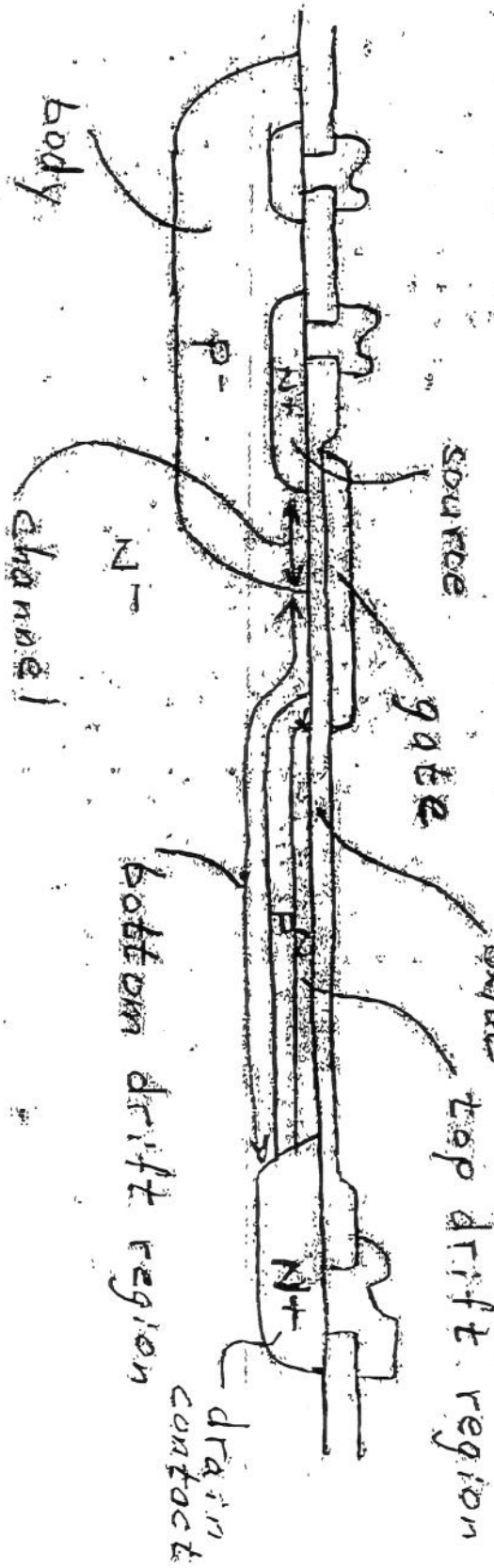
Fig 3

Lateral PNP



P channel MOS





Improved lateral Nch DMOS

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name	company/firm	tel	fax
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William J. Marsden, Jr.	FISH & RICHARDSON P.C.		(302) 652-0607

RE *Power Integrations v. Fairchild Semiconductor, et al.*

MESSAGE

Please see attached.

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